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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,647	11/12/2003	Hyoung-Joon Kim	5649-927dv	7889

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,647	KIM ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/052,721.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/12/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/706,647, which is a divisional of Application Serial No. 10/052,721 now US 6,680,511. Currently, claims 1-12 are pending.

Information Disclosure Statement

2. Since the examiner was unable to obtain from the parent application a copy of the non-patent literature reference to Klause et al., which was cited on the PTO 1449 form filed 12 November 2003, the reference has not yet been considered. It is requested that the Applicant resubmit a copy of the reference for the examiner's review along with a copy of the1449 filed on 12 November 2003, both of which may be faxed directly to the examiner.[1] The reference will be considered upon receipt.

3. The signed and dated 1449, including the initialed reference, will be mailed along with the next action.

Specification

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

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[1] The examiner's fax number is (571) 273-1846. Please call before sending the fax.

Claim Objections

5. Claim 5 is objected to because of the following informalities: "the structure" should be "the method" (claim 5, line 2). Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

6. *Claims 3, 7, 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.*

The phrase "the etchant" lacks antecedent basis (claim 3, line 2; claim 7, line 2; claim 11, lines 2 and 5).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. *Claims 1-3 and 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Cho et al. (US 6,001,719).*

The Cho et al. patent (Cho) discloses a method of fabricating a self-aligned contact structure for a microelectronic device (figs. 2A-2D and accompanying text). The method comprises: forming a conductive layer 120, 125 on a microelectronic substrate (fig. 2A and col. 3, lines 9-25); forming an insulating layer 130 on the conductive layer (fig. 2A and col. 3, lines 9-25), the insulating layer including an overhanging portion that extends beyond the conductive layer (fig. 2B); forming a sidewall insulating region 135 disposed laterally adjacent a sidewall of the conductive layer and extending between the overhanging portion of the insulating layer and the microelectronic substrate (fig. 2C and col. 3, lines 36-42); and forming a conductive region 145 disposed laterally adjacent the sidewall insulating region such that the sidewall insulating region separates the sidewall of the conductive layer and the conductive region (fig. 2D and col. 3, line 65 – col. 4, line 1).

An insulating region 115 is formed between the overhanging portion of the insulating layer and the microelectronic substrate, and an insulating sidewall spacer 140a is formed, which conforms to a sidewall of the insulating layer, the sidewall insulating region, and an adjoining surface of the insulating region (col. 3, lines 60-65). The conductive region 145 is laterally adjacent the insulating sidewall spacer (fig. 2D).

Forming the conductive layer comprises adjusting an etchant so that the insulating layer includes the overhanging portion that extends beyond the conductive layer (col. 3, lines 32-35).

8. *Claims 1, 3-5, 7, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Woo et al. (US 5,262,352).*

The Woo et al. patent (Woo) discloses a method of fabricating a self-aligned contact structure for a microelectronic device (figs. 1, 2, 15-16 and accompanying text). The method comprises: forming a conductive layer 17, 18 on a microelectronic substrate (fig. 1 and col. 4, lines 4-9); forming an insulating layer 20 on the conductive layer (fig. 1 and col. 4, lines 11-15), the insulating layer including an overhanging portion that extends beyond the conductive layer (fig. 2); forming a sidewall insulating region 22 disposed laterally adjacent a sidewall of the conductive layer and extending between the overhanging portion of the insulating layer and the microelectronic substrate (fig. 17 and col. 9, lines 26-34); and forming a conductive region 24 disposed laterally adjacent the sidewall insulating region such that the sidewall insulating region separates the sidewall of the conductive layer and the conductive region (fig. 17 and col. 5, lines 20-23).

Forming the conductive layer comprises adjusting an etchant so that the insulating layer includes the overhanging portion that extends beyond the conductive layer (col. 4, lines 33-45).

Forming the conductive layer comprises forming a conductive layer having first and second metallic layers (col. 4, lines 4-9).[2]

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[2] Whereas Woo discloses that the conductive layer 18 is preferably polysilicon, Woo also discloses that other known conductive layers may be used for conductive layer 18. In addition,

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. *Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woo et al. (US 5,262,352).*

Whereas Woo teaches forming an insulating region 16 between the overhanging portion of the insulating layer 20 and the microelectronic substrate (fig. 2), Woo does not teach forming an insulating sidewall spacer conforming to a sidewall of the insulating layer 20, the sidewall insulating region 22 and an adjoining surface of the insulating region 16, in the embodiment of figs. 1, 2, and 15-17. However, in the embodiment of figs. 1-3, Woo does teach forming an insulating sidewall spacer 22 conforming to a sidewall of the insulating layer 20 and an adjoining surface of the insulating region 16 (fig. 3 and col. 4, line 66 – col. 5, line 4). The conductive region 24 is laterally adjacent the insulating sidewall spacer (fig. 3).

Since Woo teaches that the method disclosed in the embodiment of figs. 1, 2, and 15-17 can be combined with other disclosed embodiments (col. 9,

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Woo discloses that conductive layer 18 is similar to conductive layer 14. Conductive layer 14

lines 44-47), it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of figs. 1, 2, and 15-17 by forming an insulating sidewall spacer conforming to a sidewall of the insulating layer, the sidewall insulating region, and an adjoining surface of the insulating region, as shown in the method of figs. 1-3.

10. *Claims 9, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woo in view of Huang et al. (US 6,214,715 B1).*

As discussed above, Woo discloses a method of fabricating an integrated circuit memory device, wherein the method comprises forming first and second metal lines (figs. 1, 2, 5-17 and accompanying text). Forming the first conductive structure comprises: forming a first conductive layer 17, 18 on a microelectronic substrate (fig. 1 and col. 4, lines 4-9); forming a first insulating layer 20 on the first conductive layer (fig. 1 and col. 4, lines 11-15), the first insulating layer including an overhanging portion that extends beyond the first conductive layer (fig. 2); and forming a first sidewall insulating region 22 disposed laterally adjacent a sidewall of the first conductive layer and extending between the overhanging portion of the first insulating layer and the microelectronic substrate (fig. 17 and col. 9, lines 26-34). Forming the second conductive structure comprises: forming a second conductive layer 17, 18 on a microelectronic substrate (fig. 1 and col. 4, lines 4-9); forming a second insulating layer 20 on the conductive layer (fig. 1 and col. 4, lines 11-15), the

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may be any known layer, such as metal and metal alloys (col. 3, lines 48-52).

second insulating layer including an overhanging portion that extends beyond the second conductive layer (fig. 2); and forming a second sidewall insulating region 22 disposed laterally adjacent a sidewall of the second conductive layer and extending between the overhanging portion of the second insulating layer and the microelectronic substrate (fig. 17 and col. 9, lines 26-34).

Forming the first conductive layer comprises adjusting an etchant so that the first insulating layer includes the overhanging portion that extends beyond the first conductive layer, and forming the second conductive layer comprises adjusting an etchant so that the second insulating layer includes the overhanging portion that extends beyond the second conductive layer (col. 4, lines 33-45).

Forming the first conductive layer comprises forming a conductive layer having first and second metallic layers 17, 18, and forming the second conductive layer comprises forming a conductive layer having third and fourth metallic layers 17, 18 (col. 4, lines 4-9).[3]

Whereas Woo teaches forming first and second insulating regions 16 between the overhanging portion of the first insulating layer 20 and the microelectronic substrate and between the overhanging portion of the second insulating layer 20 and the microelectronic substrate, respectively (fig. 2), Woo does not teach forming first and second insulating sidewall spacers conforming to a sidewall of the first and the second insulating layers 20, the first and

second sidewall insulating regions 22, and an adjoining surface of the first and second insulating regions 16, in the embodiment of figs. 1, 2, and 15-17. However, in the embodiment of figs. 1-3, Woo does teach forming an insulating sidewall spacer 22 conforming to a sidewall of first and second insulating layers 20 and an adjoining surface of first and the second insulating regions 16 (fig. 3 and col. 4, line 66 – col. 5, line 4).

Since Woo teaches that the method disclosed in the embodiment of figs. 1, 2, and 15-17 can be combined with other disclosed embodiments (col. 9, lines 44-47), it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of figs. 1, 2, and 15-17 by forming first and second insulating sidewall spacers conforming to a sidewall of the first and second insulating layers, the first and second sidewall insulating regions, and an adjoining surface of the first and second insulating regions, respectively, as shown in the method of figs. 1-3.

While Woo teaches that the structure formed by the method of figs. 1, 2, and 15-17 may be used in a memory device (col. 9, lines 61-64), Woo does not teach that the first and second conductive structures are first and second bit lines.

The Huang et al. patent (Huang) discloses a method for forming a self-aligned contact structure for a microelectronic device (figs. 8A-14 and accompanying text). The method comprises forming first and second

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[3] See Footnote No. 2.

conductive structures 20, which are separated by a self-aligned contact structure 55 (fig. 14). The first and second conductive structures 20 comprise first and second bit lines, respectively, in a dynamic random access memory (DRAM) (fig. 8B and col. 4, lines 34-37). The self-aligned contact 55 serves as a storage electrode for a storage capacitor in a DRAM (fig. 14 and col. 5, lines 50-52). See also col. 4, lines 28-30.

Since Woo and Huang are from the same field of endeavor, the purpose for which Huang is relied upon would have being recognized in Woo by one of ordinary skill in the art at the time the invention was made.

Since the method of Woo forms first and second conductive structures separated by a self-aligned contact 24, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Woo in view of Huang, by using the method of Woo to form a DRAM comprising a first and a second bit line separated by a storage electrode of a capacitor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMJ
22 August 2004

Mary Wilczewski
Primary Examiner